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Docket No.: 60188-756 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	Customer Number: 20277
Toyokazu FUJI	:	Confirmation Number: 8984
Serial No.: 10/799,715	:	Group Art Unit: 2811
Filed: March 15, 2004	:	Examiner: To be Assigned

For: SEMICONDUCTOR DEVICE AND PROCESS FOR FABRICATION OF THE SAME

PETITION TO MAKE SPECIAL UNDER 37 CFR § 1.102(d)

Mail Stop Petitions
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Applicant hereby petitions to make special the above-identified application in accordance with 37 CFR § 1.102(d). However, Applicant notes that the above application claims priority to U.S. Ser. No. 09/018,181 filed February 3, 1998, which is more than five years, and hence should be granted special status as set forth in MPEP 708.01 I. To the extent that special status has not already been granted to the above application, Applicant hereby petitions for such. Pursuant to MPEP § 708.02(VIII), Applicant complies with each of the following items:

A. FEE

In the event that special status has not already been granted to the above application, please charge Deposit Account 500417 the amount of $130.00 as set forth in 37 CFR § 1.17(h) to cover the fee for the present Petition to Make Special.

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B. SINGLE INVENTION

If the Office determines that all the claims presented are not obviously directed to a single invention, Applicants will make an election without traverse and hereby invites the Examiner to telephone the undersigned Applicants' representative for a telephonic election.

C. PRE-EXAMINATION SEARCH

Applicants submit that a pre-examination search has been made in prior related applications U.S. 09/536,618 filed March 28, 2000 and its parent application 09/018,181 filed February 3, 1998. The following relevant references were found:

U.S. Pat. No. 5,936,272 to Lee;

U.S. Pat. No. 5,652,165 to Lu et al.; and

U.S. Pat. No. 5,399,518 to Sim et al.

D. COPY OF THE REFERENCES

Each of the above references have been cited on an IDS filed with the above application on March 15, 2004, but copies were not provided since they are contained in the parent applications. Courtesy copies of the above references are provided with this petition.

E. DETAILED DISCUSSION

Present Invention

The present invention relates to a semiconductor using an insulating film with impurities, an interconnection and a silicon oxide film in contact with the insulating film and a silicon nitride film formed on the silicon oxide film.

As recited by pending claims 34, 43, 49 and 61, as amended in the Preliminary Amendment submitted on March 15, 2004, the present invention as illustrated for example in Figs. 1 and 2, includes:

34. (New) A semiconductor device comprising:

a substrate having a semiconductor region;

an insulating film formed over said semiconductor region, said insulating film including impurities;

an interconnection in contact with a first region of said insulating film,

a silicon oxide film in contact with a second region of said insulating film;

a silicon nitride film formed on said silicon oxide film.

43. (New) A semiconductor device comprising:

a substrate having a semiconductor region;

an insulating film formed over said semiconductor region, said insulating film including phosphorus;

an interconnection in contact with a first region of said insulating film,

a silicon oxide film in contact with a second region of said insulating film;

a silicon nitride film formed on said silicon oxide film.

49. (New) A semiconductor device comprising:

a substrate having a semiconductor region;

a gate electrode formed over said semiconductor region,

an insulating film formed over said semiconductor region, said insulating film including impurities;

a silicon oxide film formed on said insulating film;

a silicon nitride film formed on said silicon oxide film; and

wherein said insulating film is formed over said gate electrode.

61. (New) A semiconductor device comprising:

a substrate having a semiconductor region;

an insulating film formed over said semiconductor region, said insulating film including impurities;

an interconnection in contact with a first region of said silicon oxide film,

a second region of said silicon oxide film in contact with said insulating film; and

a silicon nitride film formed on said silicon oxide film.

Differences Between Claims 34 And 43

Comparison with Lee (U.S. Pat. No. 5,936,272)

Lee discloses a semiconductor device having a substrate 100, a gate line 70 formed over the substrate 100, a BPSG film as a first dielectric layer 125 formed to be substantially

planarized for an upper surface of a gate line cap 72 on the gate line 70, a TEOS film as the second dielectric layer 135 formed on the first dielectric layer 125 and the gate line cap 72, and a silicon nitride film (third dielectric layer) 136 formed on the second dielectric layer 135 (Fig. 4G).

In the semiconductor device disclosed in Lee, as illustrated in Fig. 4G, the BPSG film (first dielectric layer) 125 is formed to be substantially planarized for the upper surface of the gate line cap 72 on the gate line 70, and the O_3–TEOS film (second dielectric layer) 135 is formed on the BPSG film (first dielectric layer) 125 and the gate line cap 72. The entire upper surface of the BPSG film (first dielectric layer) 125 is in contact with the O_3–TEOS film 135. Thus, the interconnection is not contacted to the BPSG film 125.

On the other hand, in the semiconductor device recited in claim 34, as illustrated in Fig. 1, the interconnection 4 is in contact with the first region of the insulating film 3 and the silicon oxide film 5 is in contact with the second region thereof.

Comparison with Lu (U.S. Pat. 5,652,165)

Lu discloses a semiconductor device having a substrate 10, a first insulation layer 30A formed on the substrate 10, a barrier layer 32A formed on the first insulation layer 30A, and a capacitor dielectric layer 50 formed on the barrier layer 32A, wherein the entire bottom surface of the barrier layer 32A is in contact with the upper surface of the insulation layer 30A (Fig. 11). More specifically, the first insulation layer 30A is formed of silicon oxide or silicon nitride, more preferably doped or undoped silicon oxide such as TEOS oxide, BPSG or PSG. The barrier layer 32A is formed of silicon oxide or silicon nitride, more preferably of a silicon nitride layer. The capacitor dielectric layer 50 is composed of a three layer structure of silicon oxide/silicon

nitride/silicon oxide (ONO), a two layer structure of silicon oxide/silicon nitride (ON), or silicon nitride.

As illustrated in Fig. 11, Lu discloses that the barrier layer 32A formed of silicon nitride is formed on the insulation layer 30A such as TEOS oxide, BPSG or PSG. In other words, silicon nitride is formed directly on BPSG or PSG.

On the other hand, in the semiconductor device recited in claim 34, as illustrated in Fig. 1, the silicon oxide film 5 is formed between the insulating layer 3 and the silicon nitride film 6.

Moreover, Lu discloses that the barrier layer 32A is formed on the entire surface of the insulation layer 30A. Thus, the interconnection is not in contact with the insulation layer 30A.

Comparison with Sim (U.S. Pat. No. 5,399,518)

Sim discloses a semiconductor device having a substrate 10, a planarization layer (BPSG or PSG) 22 formed over the semiconductor substrate 10, an etching stop layer 42 formed on the planarization layer 22, a high temperature oxide (HTO) first 44 formed on the etching stop layer 22, a contact hole formed by penetrating the HTO 44, the etching stop layer and the planarization layer 22, and a contact electrode formed within the contact hole (Fig. 5).

Sim discloses, as illustrated in Fig. 9, that the etching stop layer (silicon nitride) 42 is formed directly on the planarization layer (PSG, BPSG) 22. Thus, the silicon oxide film is not formed between the planarization layer 22 and the silicon nitride 42.

Moreover, Sim discloses the etching stop layer 42 is formed on the entire upper surface of the planarization layer 22. Thus, the interconnection is not in contact with the planarization layer 22.

Differences Between Claim 49

Comparison with Lee (U.S. Pat. No. 5,936,272)

Lee discloses, a semiconductor device, as illustrated in Fig. 4G, in which the BPSG film (first dielectric layer) 125 is formed to be substantially planarized for the upper surface of the gate line cap 72 on the gate line 70, and the O_3–TEOS film (second dielectric layer) 135 is formed on the BPSG film (first dielectric layer) 125 and the gate line cap 72. Thus, the BPSG film (first dielectric layer) 125 is not formed on the gate line 70.

On the other hand, in the semiconductor device recited in claim 49, as illustrated in Fig. 1, the insulating film 3 is formed on the gate electrode 2.

Comparison with Lu (U.S. Pat. 5,652,165)

As illustrated in Fig. 11, Lu discloses as the best mode that the barrier layer 32A formed of silicon nitride is formed on the insulation layer 30A such as TEOS oxide, BPSG or PSG. In other words, silicon nitride is formed directly on BPSG or PSG.

On the other hand, in the semiconductor device recited in claim 49, the silicon oxide film 5 is formed between the insulating film 3 and the silicon nitride film 6.

Comparison with Sim (U.S. Pat. No. 5,399,518)

Sim discloses, as illustrated in Fig. 9, that the etching stop layer (silicon nitride) 42 is formed directly on the planarization layer (PSG, BPSG) 22. Thus, the silicon oxide film is not formed between the planarization layer 22 and the silicon nitride 42.

Differences Between Claim 61

Comparison with Lee (U.S. Pat. No. 5,936,272)

Lee discloses, a semiconductor device, as illustrated in Fig. 4G, in which the BPSG film (first dielectric layer) 125 is formed to be substantially planarized for the upper surface of the gate line cap 72 on the gate line 70, and the O_3–TEOS film (second dielectric layer) 135 is formed on the BPSG film (first dielectric layer) 125 and the gate line cap 72. The entire upper surface of the BPSG film (first dielectric layer) 125 is in contact with the O_3–TEOS film 135. Thus, the interconnection is not contacted to the BPSG film 125.

On the other hand, in the semiconductor device recited in claim 61, as illustrated in Fig. 1, the interconnection 4 is in contact with the first region of the silicon oxide film 5, and the insulating film 3 is in contact with the second region thereof.

Comparison with Lu (U.S. Pat. 5,652,165)

As illustrated in Fig. 11, Lu discloses as the best mode that the barrier layer 32A formed of silicon nitride is formed on the insulation layer 30A such as TEOS oxide, BPSG or PSG. In other words, silicon nitride is formed directly on BPSG or PSG. Hence, Lu fails to disclose the interconnection and the silicon oxide film of the present invention.

Comparison with Sim (U.S. Pat. No. 5,399,518)

Sim discloses, as illustrated in Fig. 9, that the etching stop layer (silicon nitride) 42 is formed directly on the planarization layer (PSG, BPSG) 22. Thus, the silicon nitride 42 is formed directly on the planarization layer 22. Hence, Sim fails to disclose the interconnection and the silicon oxide film of the present invention.

Thus, it is respectfully submitted that each of the above references, taken alone or in combination, fails to disclose or suggest at least the foregoing elements recited by the pending claims. Accordingly, for all of the foregoing reasons, it is respectfully submitted that the pending claims are patentable over the foregoing references.

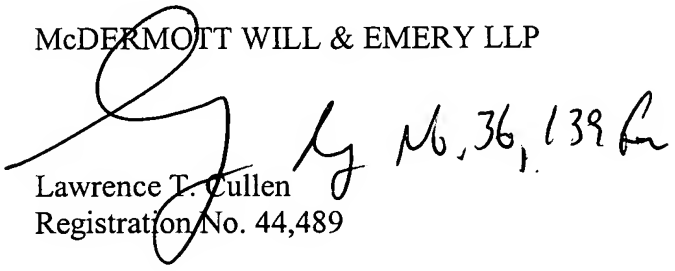
F. CONCLUSION

In view of the above, it is urged that the petition to make special is in proper form, and an indication of grant is respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



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